CLAIMS

WHAT IS CLAIMED:

1. A transistor, comprising:

a substrate;

an active region defined in said substrate;

a gate insulation layer formed above said active region; and

a gate electrode formed above said gate insulation layer, said gate electrode having a middle portion located over the active region, said middle portion having a gate length and a gate height, wherein a cross-sectional area in a plane defined by said gate length and said gate height of the middle portion exceeds a value obtained by multiplying the gate length by the gate height.

2. The transistor of claim 1, wherein a lower part of said middle portion has a cross-sectional area in the plane defined by the gate length and the gate height that is substantially rectangular.

3. The transistor of claim 2, wherein an extension of an upper part of said middle portion along the gate length direction decreases from bottom to top of said upper part.

4. The transistor of claim 1, wherein the gate length is 100 nm or less.

5. The transistor of claim 1, wherein sidewalls of the lower part are, at least partially, covered by thermally grown silicon dioxide.

6. The transistor of claim 1, wherein the gate electrode comprises polycrystalline silicon and a metal.

7. The transistor of claim 1, wherein the upper part comprises a metal.

8. The transistor of claim 1, wherein the substrate is a semiconductor substrate.

9. The transistor of claim 1, wherein the substrate is an insulating substrate, and the active region is formed in a semiconductor layer deposited over the insulating substrate.

10. A method of manufacturing a field effect transistor having an improved signal performance, the method comprising:

providing a substrate and defining an active region therein;

forming a gate insulation layer over the active region;

depositing a first gate electrode material layer having a first thickness and patterning a first portion of a gate electrode, the first portion having a height substantially equal to the first thickness;

depositing an insulating layer having a thickness determined by the first thickness;

planarizing the insulating layer to expose a surface of the first portion;

selectively removing material of the planarized insulating layer so as to reduce the thickness of the insulating layer until a predefined adjustment thickness is obtained to partially expose sidewalls of the first portion;

depositing a second gate electrode material layer over the insulating layer and the first portion; and

anisotropically etching the second gate electrode material layer to form a gate electrode including the first portion and an extension portion laterally extending beyond the first portion, wherein a cross-sectional shape of the extension portion is determined by the adjustment thickness.

11. The method of claim 10, wherein the first gate electrode material layer and the second gate material layer comprise polycrystalline silicon.

12. The method of claim 11, further comprising depositing a metal layer over the gate electrode and initiate a chemical reaction of the metal layer and the polycrystalline silicon.

13. The method of claim 10, wherein the first thickness is in the range from 1-2.5 μm.

14. The method of claim 10, wherein the insulating layer comprises at least one of silicon dioxide and silicon nitride.

15. The method of claim 10, wherein selectively removing material of the insulating layer comprises using a slow chemical etch solution that is highly selective with respect to the first gate electrode material layer.

16. The method of claim 10, wherein selectively removing material of the insulating layer comprises forming one or more etch stop layers on the first portion prior to depositing the insulating layer.

17. The method of claim 16, wherein at least one of the one or more etch stop layers comprises thermally grown silicon dioxide, wherein a thickness of the thermally grown silicon dioxide affects the shape of the extension portion.

18. The method of claim 17, further comprising removing the one or more etch stop layers prior to depositing the second gate electrode material layer.

19. The method of claim 17, wherein the insulating layer comprises silicon nitride.

20. The method of claim 16, wherein at least one of the one or more etch stop layers is formed by ion implantation.

21. The method of claim 10, wherein depositing the second gate electrode material layer comprises depositing two or more layers.

22. The method of claim 21, wherein the two or more gate electrode material layers comprise different materials.

23. The method of claim 22, wherein one of the two or more gate electrode material layers comprises a metal.

24. The method of claim 10, wherein the substrate is a semiconductor substrate.

25. The method of claim 10, wherein the substrate is an insulating substrate and the method further comprises forming a layer of active material over the insulating substrate.

26. The method of claim 10, wherein the extension portion is used as an implantation mask during formation of the drain and source.